



MS-7508Ver:10

CPU:

AMD AM2 and AM2R2

System Chipset:

NVIDIA MCP78U/S

On Board Chipset:

Winbond Super I/O -- FINTEK71882

LAN -- RTL8211BL

HD Codec --ALC888

JIMCRO 1394

BIOS -- SPI ROM

Main Memory:

DDR 2*4(Max4GB)

Expansion Slots:

PCI 2.3 Slot *2

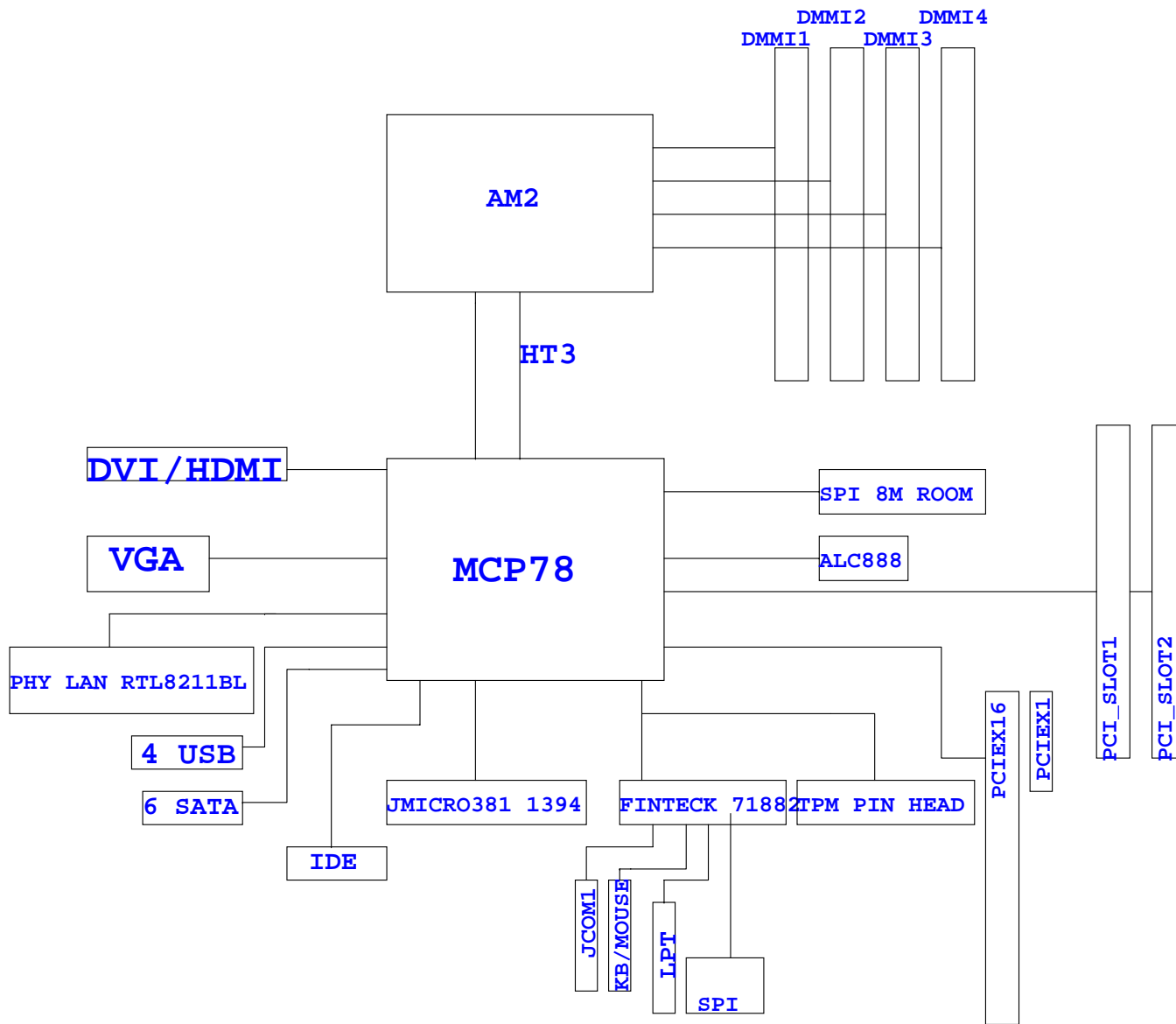
PWM:

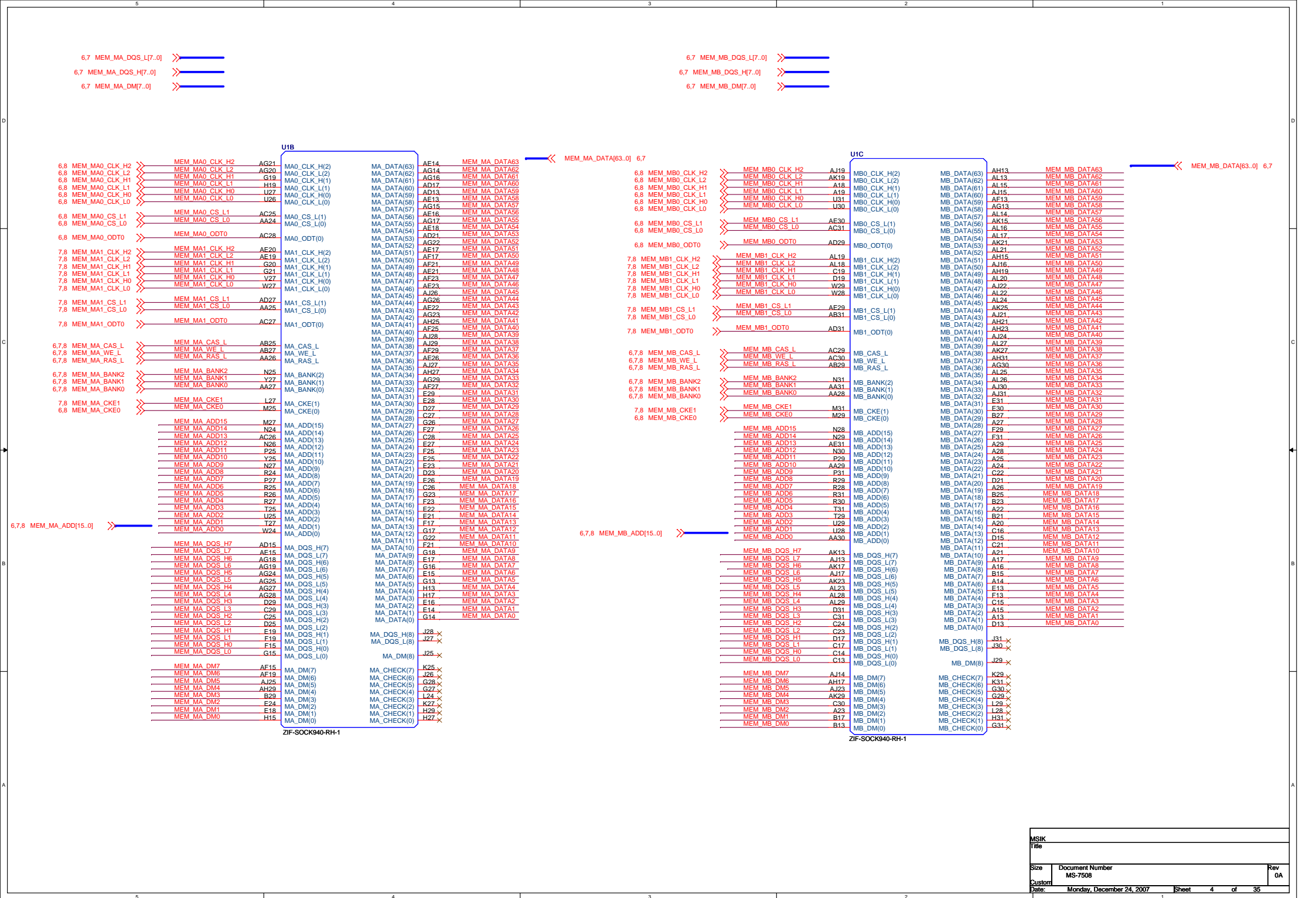
ST6740+ST6741

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NOTE:

all the 0ohm resistor default not stuff ,change footprint as R0402_6 or R0603_10 ,for costdown request





4.7 MEM_MA_DQS_H[7..0]
4.7 MEM_MA_DQS_L[7..0]
4.7 MEM_MA_DATA[83..0] 4.7
4.7 MEM_MA_DM[7..0]

VCC_DDR
C102
X_C0.1u16Y0402

VCC3
C103
X_C0.1u16Y0402

4.7 MEM_MB_DQS_H[7..0]
4.7 MEM_MB_DQS_L[7..0]
MEM_MB_DM[7..0] 4.7
MEM_MB_DATA[63..0] 4.7
MEM_MB_ADD[15..0] 4.7.8

VCC_DDR

VCC3
C101
C0.1u16Y0402

MEM_MA_DATA0 3
MEM_MA_DATA1 4
MEM_MA_DATA2 5
MEM_MA_DATA3 6
MEM_MA_DATA4 122
MEM_MA_DATA5 123
MEM_MA_DATA6 128
MEM_MA_DATA7 129
MEM_MA_DATA8 130
MEM_MA_DATA9 131
MEM_MA_DATA10 21
MEM_MA_DATA11 22
MEM_MA_DATA12 131
MEM_MA_DATA13 132
MEM_MA_DATA14 140
MEM_MA_DATA15 141
MEM_MA_DATA16 24
MEM_MA_DATA17 30
MEM_MA_DATA18 31
MEM_MA_DATA19 143
MEM_MA_DATA20 144
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MEM_MA_DATA23 34
MEM_MA_DATA24 35
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MEM_MA_DATA27 40
MEM_MA_DATA28 41
MEM_MA_DATA29 153
MEM_MA_DATA30 154
MEM_MA_DATA31 159
MEM_MA_DATA32 80
MEM_MA_DATA33 81
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MEM_MA_DATA35 87
MEM_MA_DATA36 88
MEM_MA_DATA37 200
MEM_MA_DATA38 201
MEM_MA_DATA39 206
MEM_MA_DATA40 89
MEM_MA_DATA41 90
MEM_MA_DATA42 95
MEM_MA_DATA43 96
MEM_MA_DATA44 208
MEM_MA_DATA45 209
MEM_MA_DATA46 214
MEM_MA_DATA47 215
MEM_MA_DATA48 98
MEM_MA_DATA49 99
MEM_MA_DATA50 107
MEM_MA_DATA51 108
MEM_MA_DATA52 217
MEM_MA_DATA53 218
MEM_MA_DATA54 226
MEM_MA_DATA55 227
MEM_MA_DATA56 234
MEM_MA_DATA57 111
MEM_MA_DATA58 116
MEM_MA_DATA59 117
MEM_MA_DATA60 229
MEM_MA_DATA61 230
MEM_MA_DATA62 236
MEM_MA_DATA63 237

MEM_MA_DQS_H0 7
MEM_MA_DQS_H1 16
MEM_MA_DQS_L1 26
MEM_MA_DQS_L2 27
MEM_MA_DQS_H3 37
MEM_MA_DQS_H4 38
MEM_MA_DQS_H5 84
MEM_MA_DQS_L4 83
MEM_MA_DQS_H6 84
MEM_MA_DQS_L6 85
MEM_MA_DQS_L5 86
MEM_MA_DQS_H7 104
MEM_MA_DQS_L7 105
MEM_MA_ADD0 188
MEM_MA_ADD1 183
MEM_MA_ADD2 182
MEM_MA_ADD3 61
MEM_MA_ADD4 60
MEM_MA_ADD5 160
MEM_MA_ADD6 161
MEM_MA_ADD7 179
MEM_MA_ADD8 177
MEM_MA_ADD9 170
MEM_MA_ADD10 57
MEM_MA_ADD11 176
MEM_MA_ADD12 196
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MEM_MA_ADD14 173
MEM_MA_ADD15 173
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MEM_MA_BANK2 73
MEM_MA_BANK3 74
MEM_MA_BANK4 192
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MEM_MA_DM2 135
MEM_MA_DM3 146
MEM_MA_DM4 155
MEM_MA_DM5 203
MEM_MA_DM6 211
MEM_MA_DM7 223
MEM_MA_DM8 224
MEM_MA_DM9 233
MEM_MA_DM10 164
MEM_MA_DM11 165
MEM_MA_DM12 166
MEM_MA_DM13 167
MEM_MA_DM14 168
MEM_MA_DM15 169
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MEM_MA_DM79 233
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MEM_MA_DM81 235
MEM_MA_DM82 236
MEM_MA_DM83 237

MEM_MA_ADD[15..0] 4.7.8

MEM_MB_DATA0 3
MEM_MB_DATA1 4
MEM_MB_DATA2 5
MEM_MB_DATA3 6
MEM_MB_DATA4 122
MEM_MB_DATA5 123
MEM_MB_DATA6 128
MEM_MB_DATA7 129
MEM_MB_DATA8 130
MEM_MB_DATA9 131
MEM_MB_DATA10 21
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MEM_MB_DATA47 215
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MEM_MB_DATA50 107
MEM_MB_DATA51 108
MEM_MB_DATA52 217
MEM_MB_DATA53 218
MEM_MB_DATA54 226
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MEM_MB_DATA56 234
MEM_MB_DATA57 111
MEM_MB_DATA58 116
MEM_MB_DATA59 117
MEM_MB_DATA60 229
MEM_MB_DATA61 230
MEM_MB_DATA62 236
MEM_MB_DATA63 237

MEM_MB_DQS_H0 7
MEM_MB_DQS_H1 16
MEM_MB_DQS_L1 26
MEM_MB_DQS_L2 27
MEM_MB_DQS_H3 37
MEM_MB_DQS_H4 38
MEM_MB_DQS_H5 84
MEM_MB_DQS_L4 83
MEM_MB_DQS_H6 84
MEM_MB_DQS_L6 85
MEM_MB_DQS_L5 86
MEM_MB_DQS_H7 104
MEM_MB_DQS_L7 105
MEM_MB_ADD0 188
MEM_MB_ADD1 183
MEM_MB_ADD2 182
MEM_MB_ADD3 61
MEM_MB_ADD4 60
MEM_MB_ADD5 160
MEM_MB_ADD6 161
MEM_MB_ADD7 179
MEM_MB_ADD8 177
MEM_MB_ADD9 170
MEM_MB_ADD10 57
MEM_MB_ADD11 176
MEM_MB_ADD12 196
MEM_MB_ADD13 174
MEM_MB_ADD14 173
MEM_MB_ADD15 173
MEM_MB_BANK0 180
MEM_MB_BANK1 181
MEM_MB_BANK2 73
MEM_MB_BANK3 74
MEM_MB_BANK4 192
MEM_MB_DM0 125
MEM_MB_DM1 126
MEM_MB_DM2 135
MEM_MB_DM3 146
MEM_MB_DM4 155
MEM_MB_DM5 203
MEM_MB_DM6 211
MEM_MB_DM7 223
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MEM_MB_DM68 222
MEM_MB_DM69 223
MEM_MB_DM70 224
MEM_MB_DM71 225
MEM_MB_DM72 226
MEM_MB_DM73 227
MEM_MB_DM74 228
MEM_MB_DM75 229
MEM_MB_DM76 230
MEM_MB_DM77 231
MEM_MB_DM78 232
MEM_MB_DM79 233
MEM_MB_DM80 234
MEM_MB_DM81 235
MEM_MB_DM82 236
MEM_MB_DM83 237

ADDRESS A0

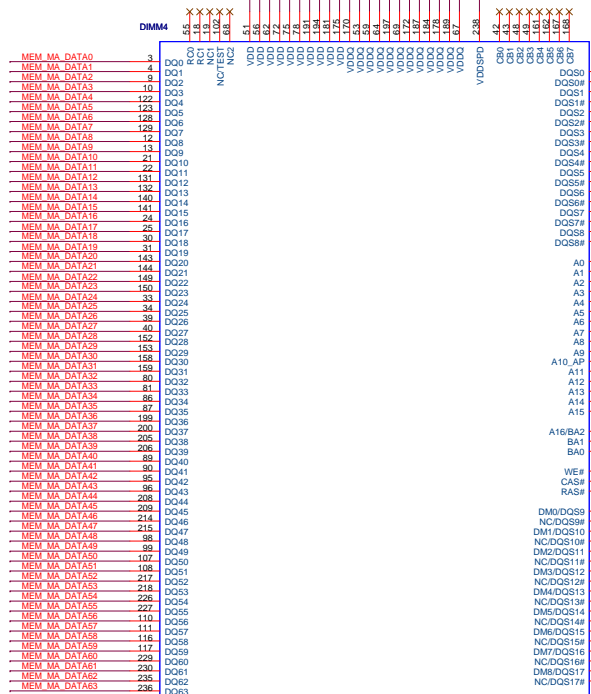
ODT0 195
ODT1 177
CKE0 52
CKE1 171
CS0# 193
CS1# 171
CK0(DU) 186
CK0(DU) 186
CK1(CK0) 137
CK1(CK0) 138
CK2(DU) 220
CK2(DU) 221
VREF 1
X1 239
SA0 240
SA1 101
X2 2
X3 3
DDR1-240_ORANG-RH

VCC_DDR
R29
C105
X_C0.1u16Y0402
VDDR_VREF
D41
D40
R31
R32
X_OR0402
X_OR0402

ADDRESS A2

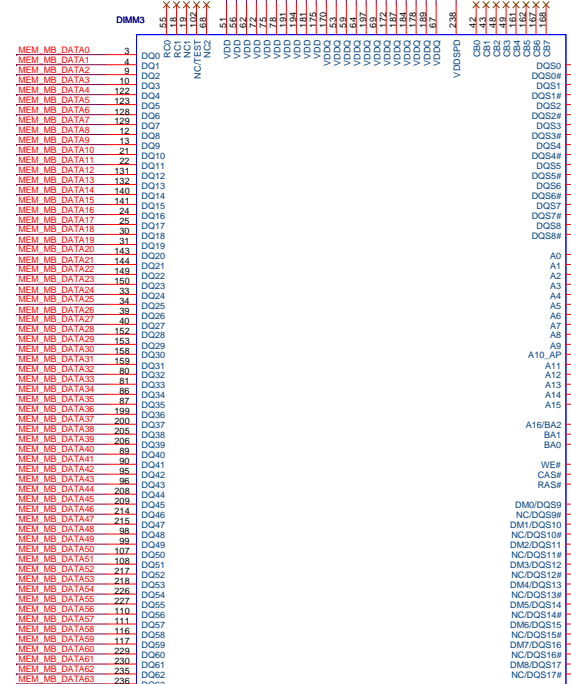
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ODT1 177
CKE0 52
CKE1 171
CS0# 193
CS1# 171
CK0(DU) 186
CK0(DU) 186
CK1(CK0) 137
CK1(CK0) 138
CK2(DU) 220
CK2(DU) 221
VREF 1
X1 239
SA0 240
SA1 101
X2 2
X3 3
DDR1-240_ORANG-RH

4.6 MEM_MA_DM[7..0] >>
4.6.8 MEM_MA_ADD[15..0] >>
4.6 MEM_MA_DQS_H[7..0] >>
4.6 MEM_MA_DQS_L[7..0] >>
4.6 MEM_MA_DATA[63..0] >>

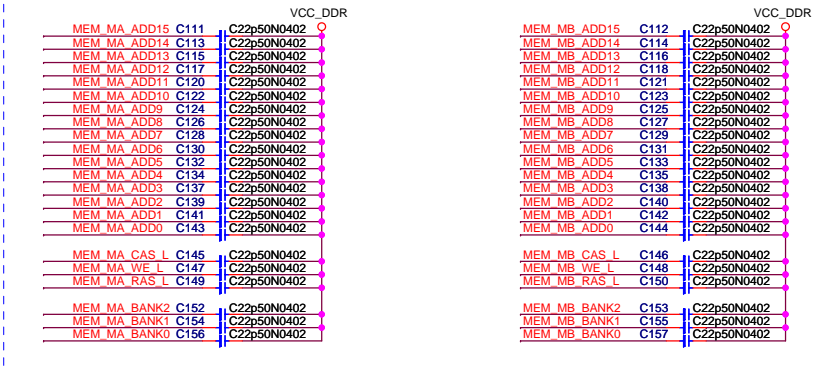
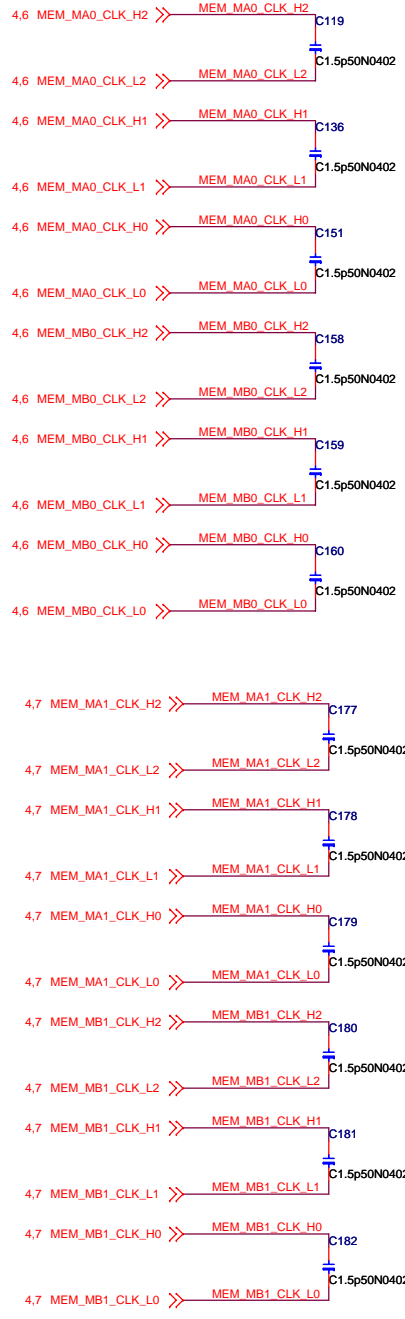
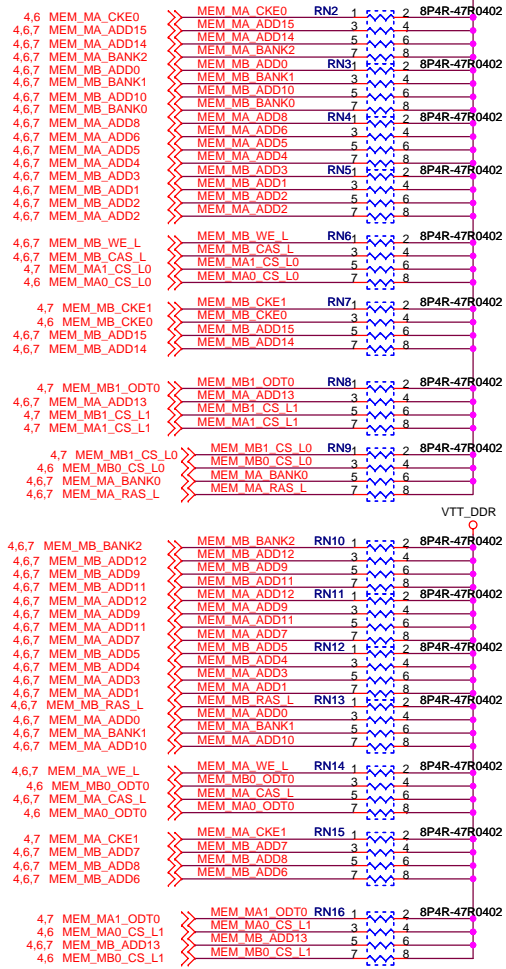


ADDRESS A4

4.6 MEM_MB_DM[7..0] >>
4.6.8 MEM_MB_ADD[15..0] >>
4.6 MEM_MB_DATA[63..0] >>

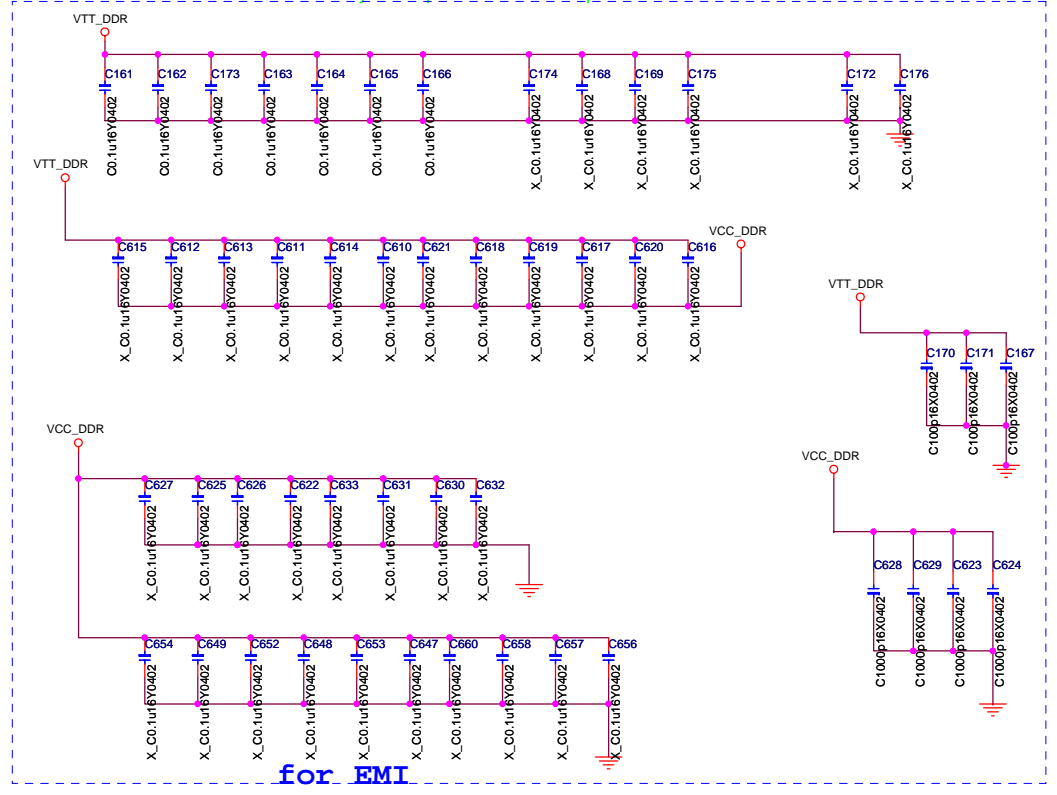


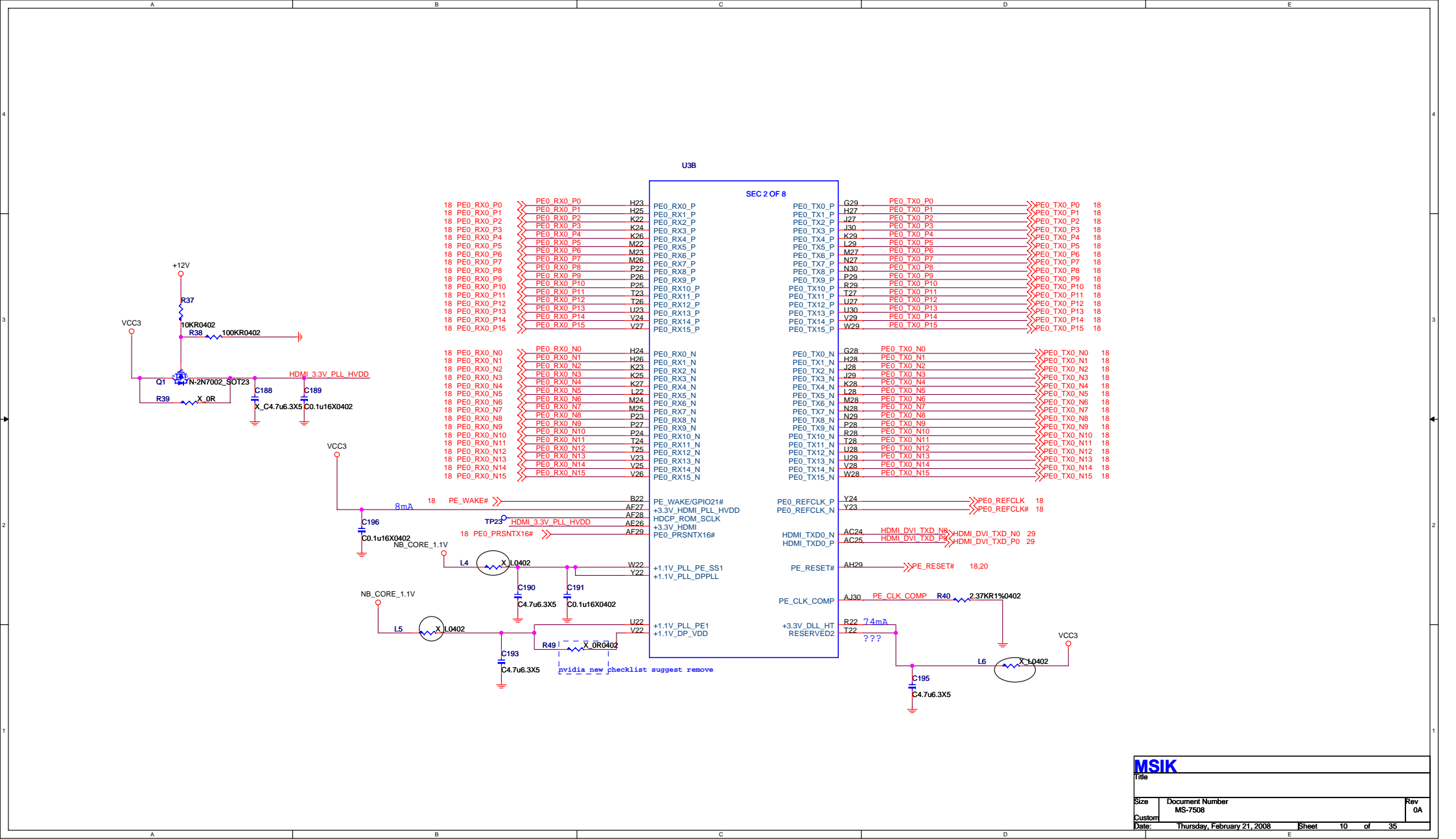
ADDRESS A6



Decoupling Between Processor and DIMMs

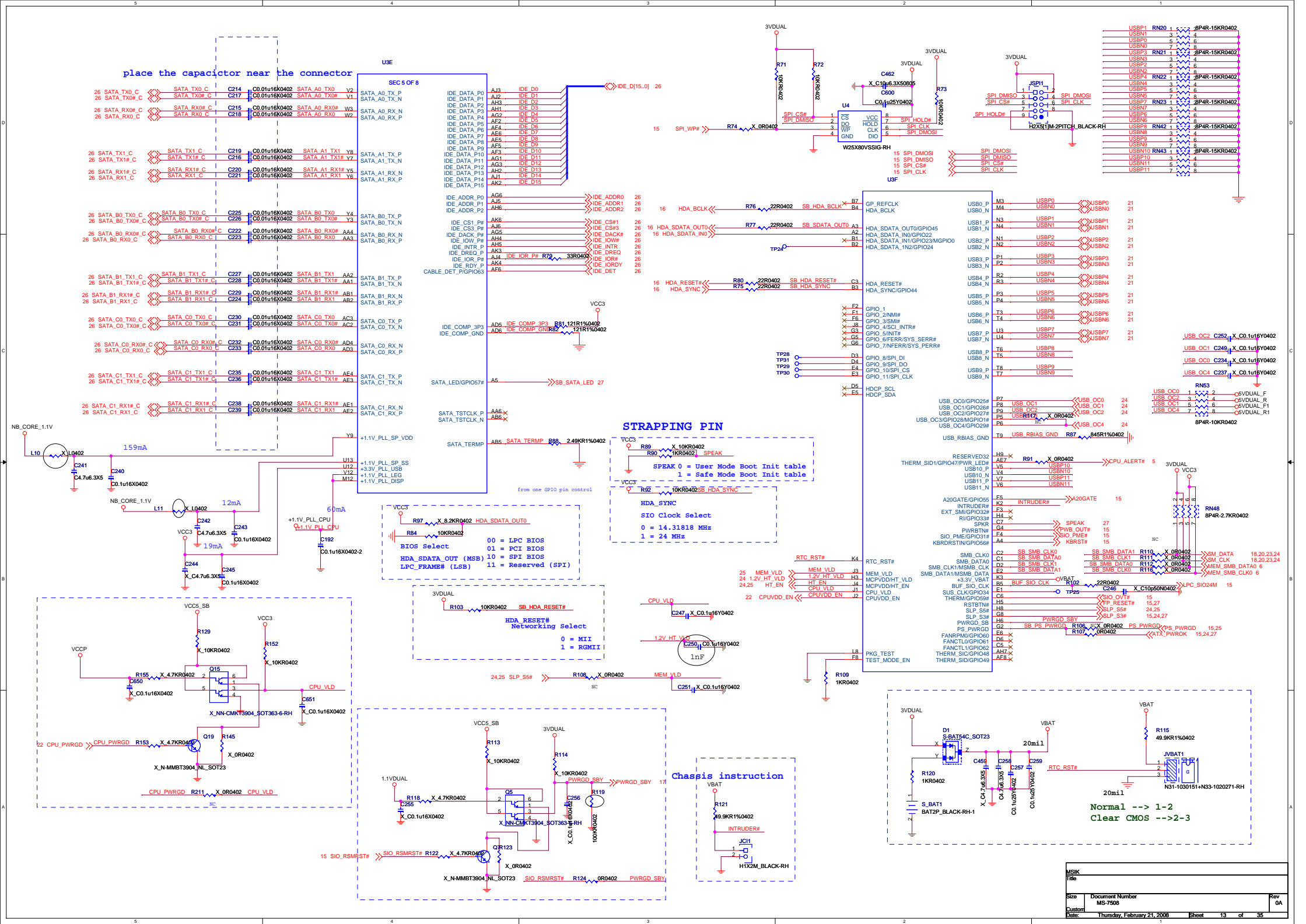
Layout: Spread out on VTT pour

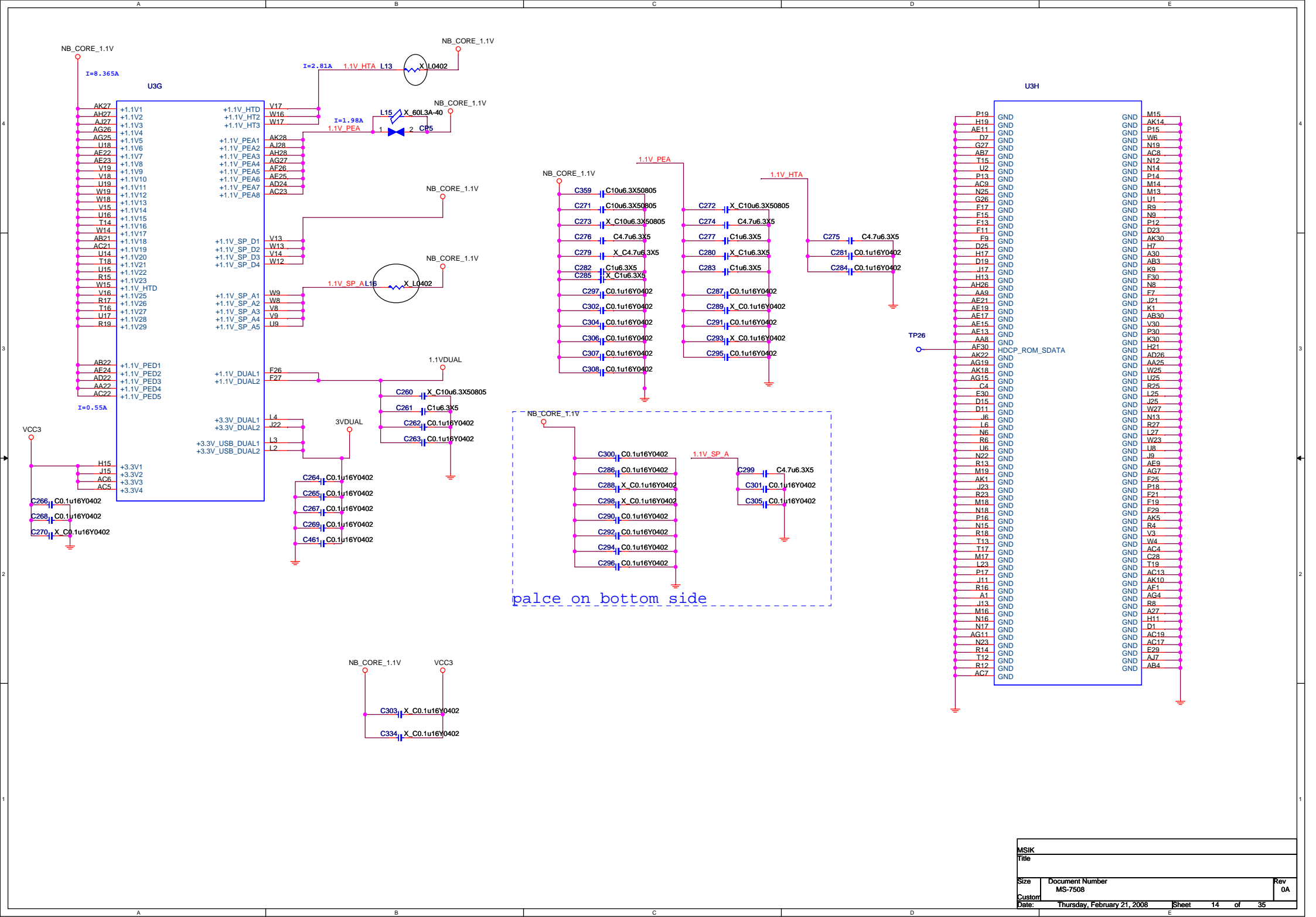


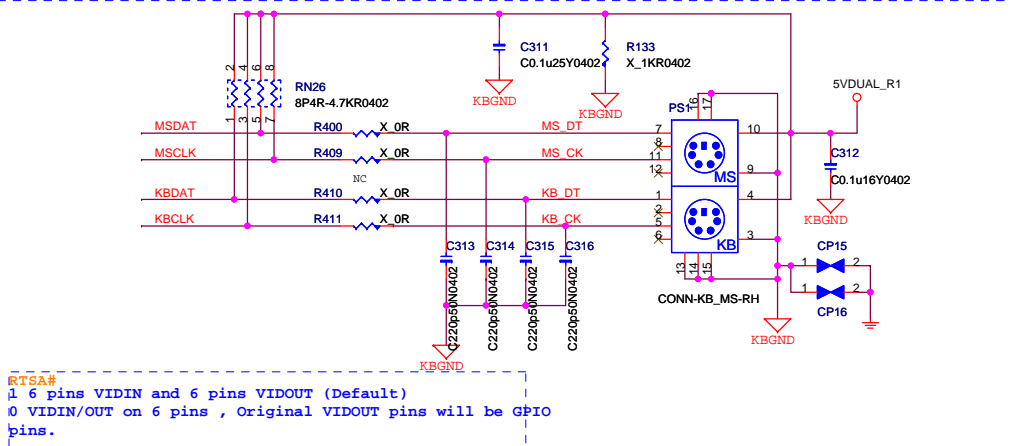
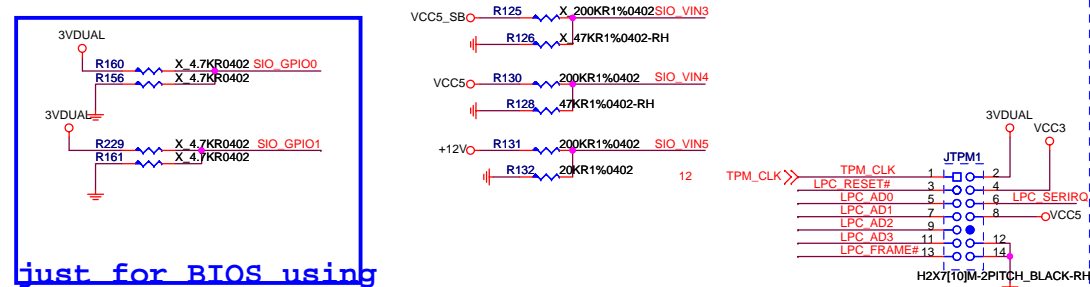


AD[31..0] <<> AD[31..0] 19
PCI_CBE#[3..0] <<> PCI_CBE#[3..0] 19

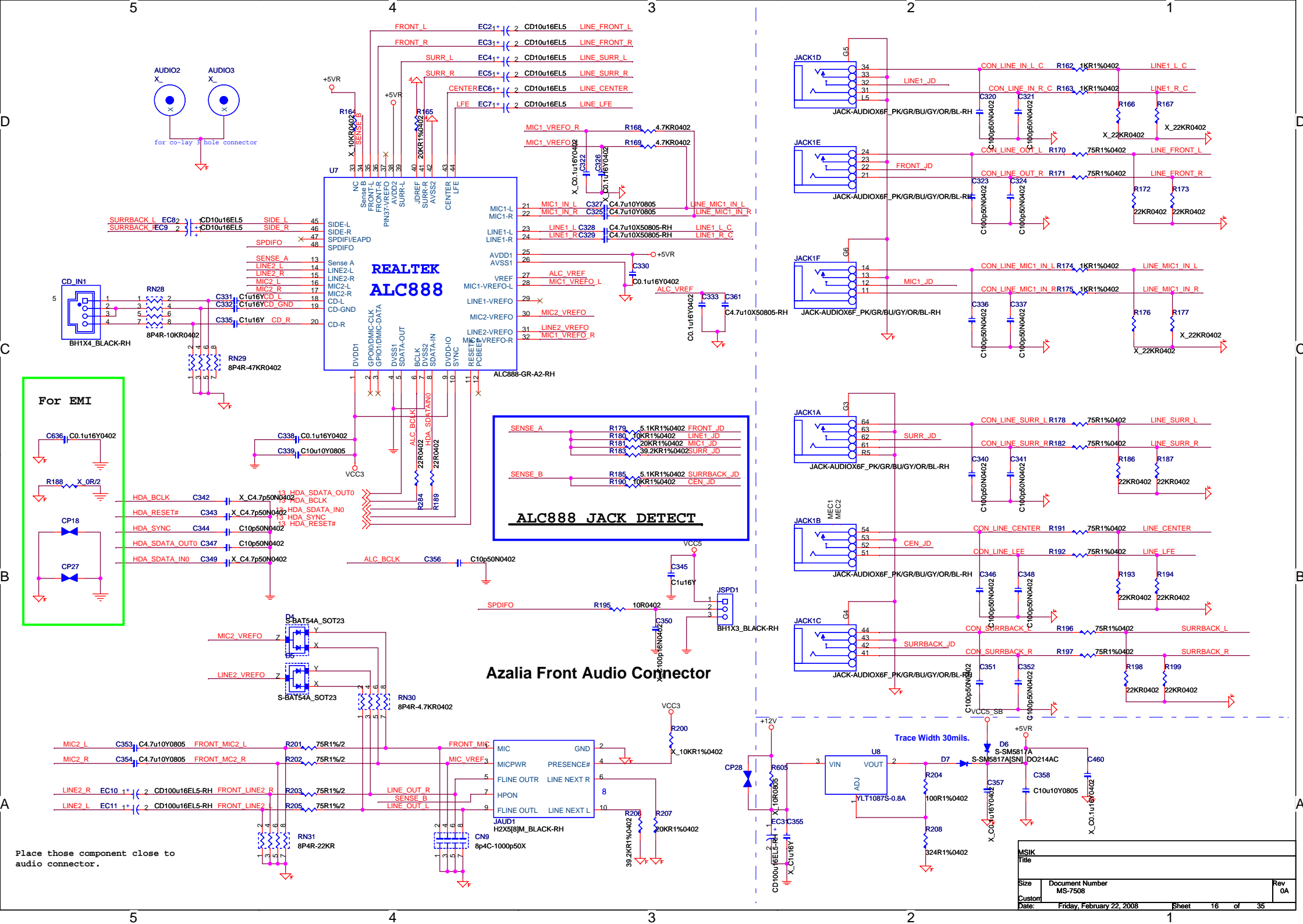






[illegible]

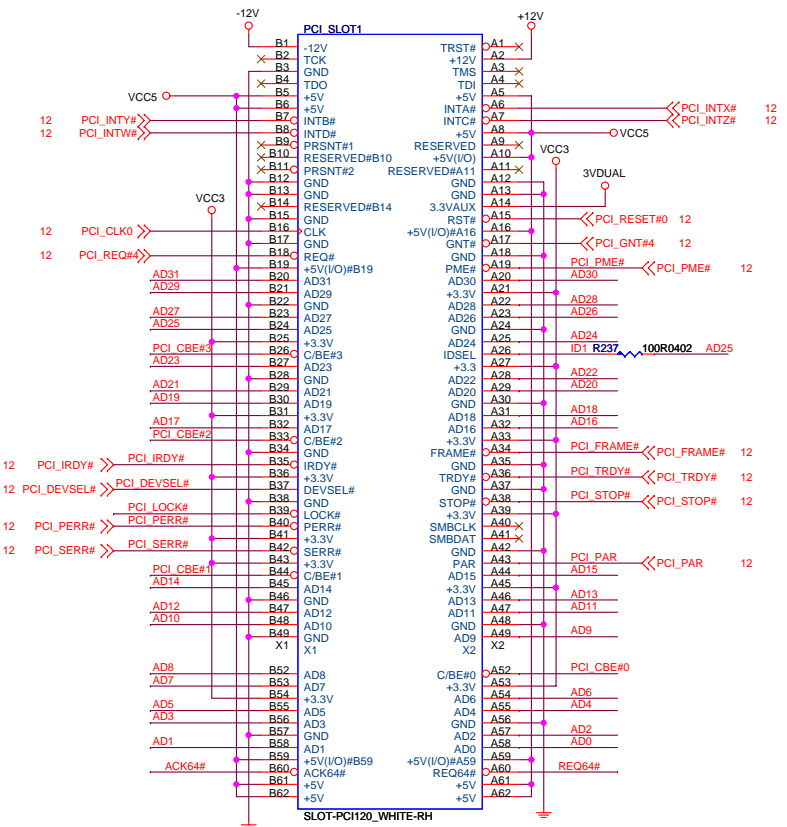
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	MS-7508		0A
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			Rev 0A

12 AD[31..0] >> AD[31..0]
12 PCI_CBE#[3..0] >> PCI_CBE#[3..0]

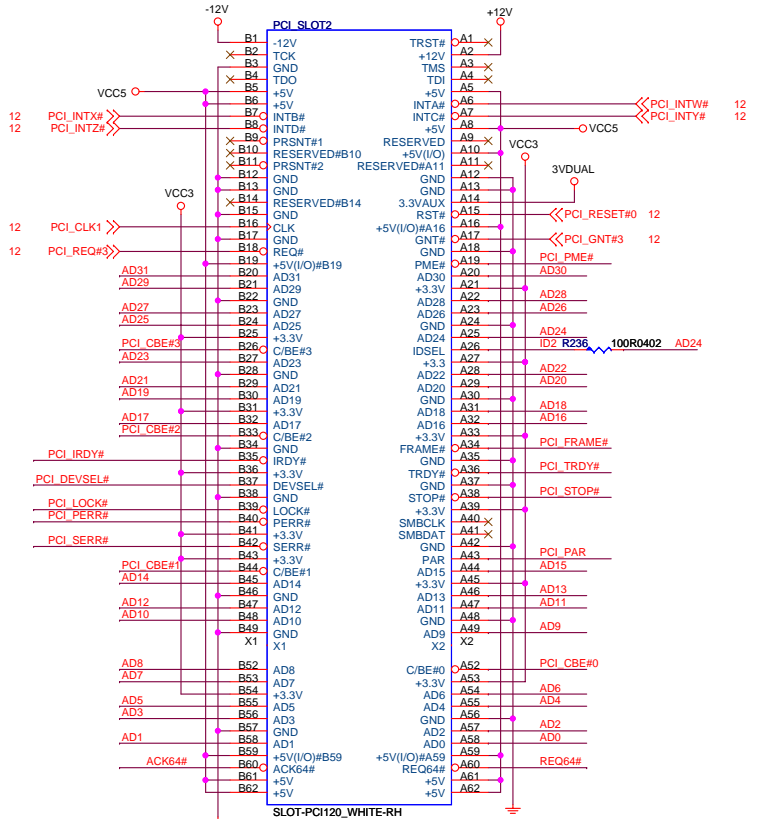
PCI SLOT 1 (PCI VER: 2.3 COMPLY)



IDSEL = AD25
MASTER = PCI_REQ#4
PCI_GNT#4

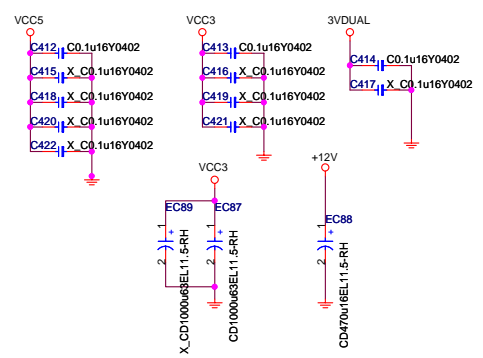
12 AD[31..0] >> AD[31..0]
12 PCI_CBE#[3..0] >> PCI_CBE#[3..0]

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

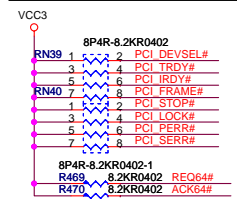


IDSEL = AD24
MASTER = PCI_REQ#3
PCI_GNT#3

PCI SLOT DECOUPLING CAPACITORS



PCI PULL-UP / DOWN RESISTORS



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The schematic diagram illustrates the internal components and connections of the JMB381 module. Key components include:

- Microcontroller:** JMB381 (B07-HB38104-J35) is the central component, shown with its pinout and internal logic.
- Power Management:**
 - VCC1_8, VCC3, and AVCC3 are power supply pins.
 - CP24, CP25, and CP26 are capacitors connected to the power supply lines.
 - L18, L19, and L20 are inductors connected to the power supply lines.
 - R266 and R267 are resistors connected to the power supply lines.
- Signal Processing:**
 - PE1394_RXP, PE1394_RXN, PE1394_TXP, and PE1394_TXN are signal pins.
 - CK_PE_100M_1394P and CK_PE_100M_1394N are clock signal pins.
 - PE_RESET# is a reset signal pin.
 - SEEDAT and SEECKL are data and clock signal pins.
 - GPIO0, GPIO1, GPIO2, and GPIO3 are general-purpose input/output pins.
 - TXIN and TXOUT are serial communication pins.
- Other Components:**
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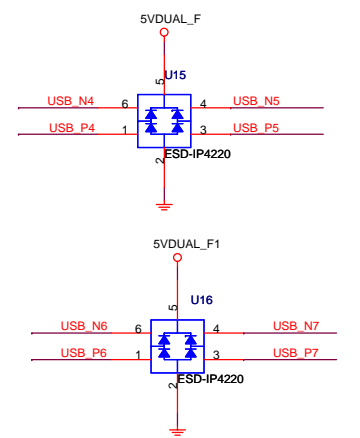
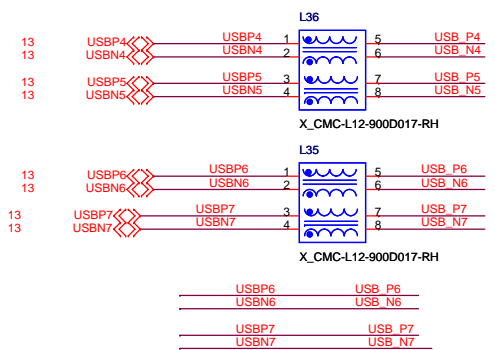
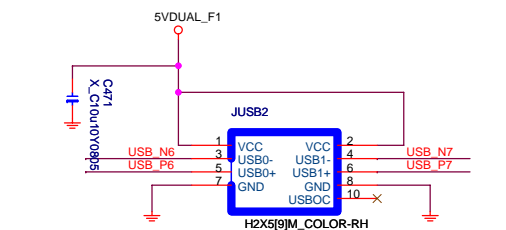
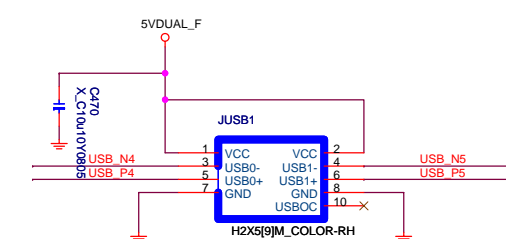
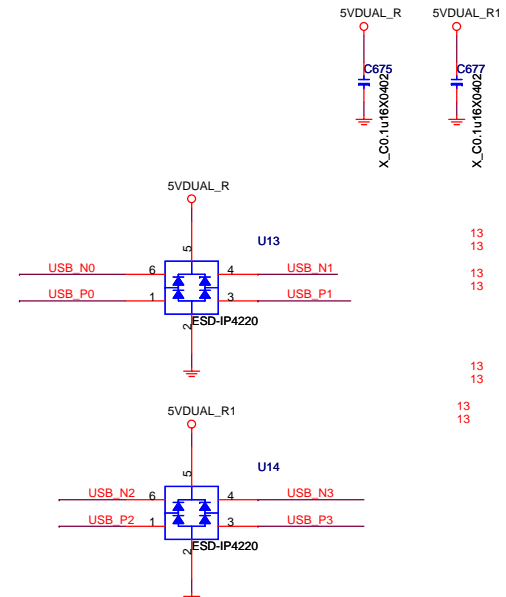
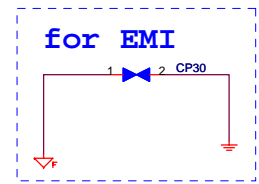
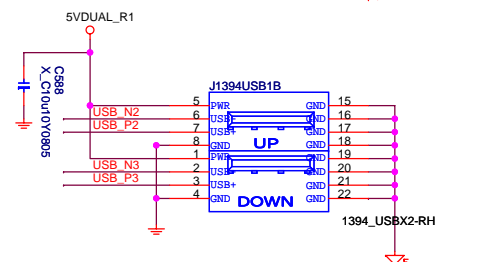
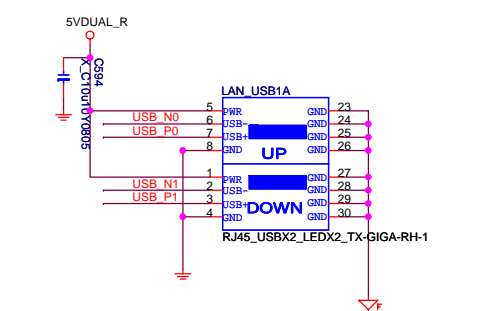
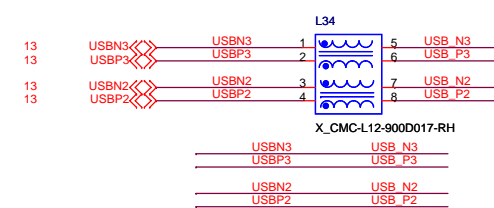
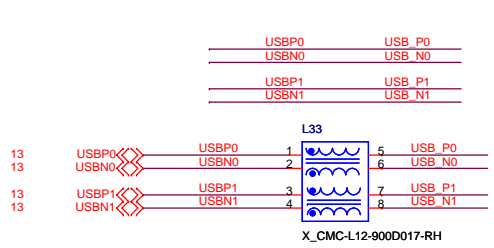
1.5A (60 mils)

Left Diagram: Internal circuitry for the H25x59M_GREEN-RH module. It shows a +12V input connected to a diode D11 (S-SS24A-TG) and a resistor F2 (S-SMD1812P150T/24-RH). The circuit includes capacitors EC50, C438, and C0.01u16X0402. The output is connected to the J1394 pinheader.

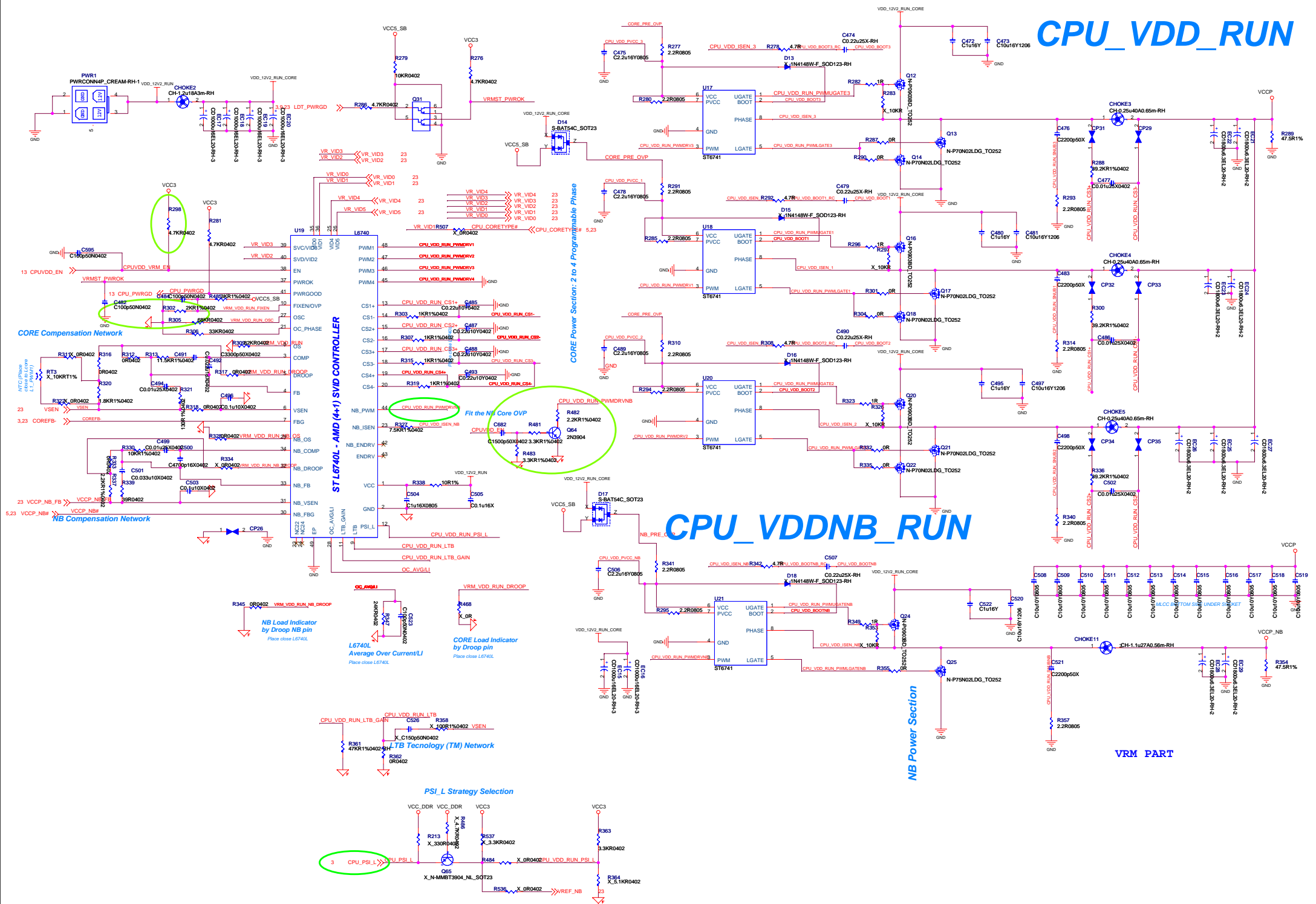
Right Diagram: Connection to the TPB1+ and TPB1- pins. It shows a diode D12 (X_ESD-IP4220) and a VCC5 connection. The circuit is connected to the TPB1+ and TPB1- pins.

For Internal 1394 pinheader

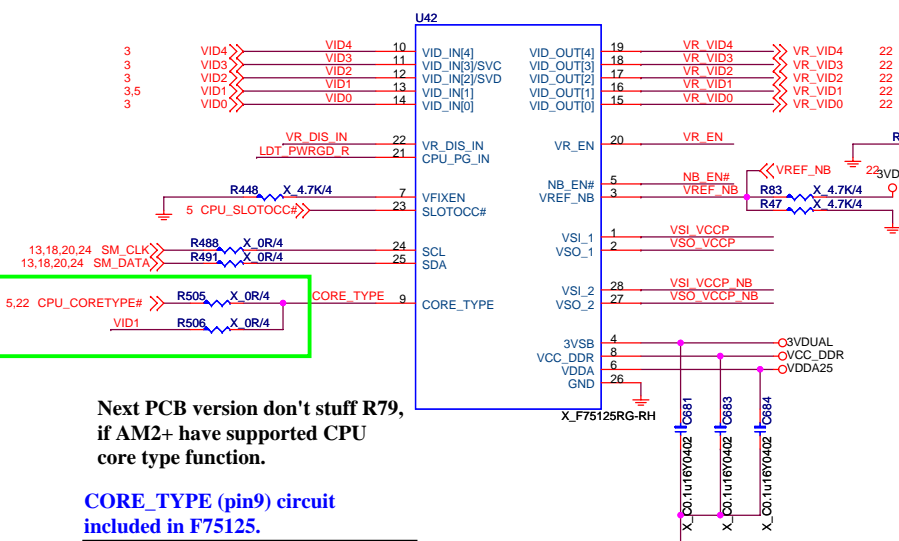
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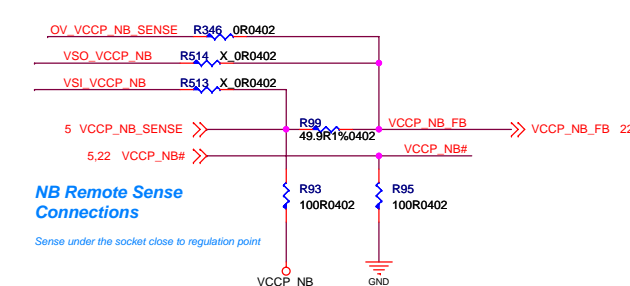
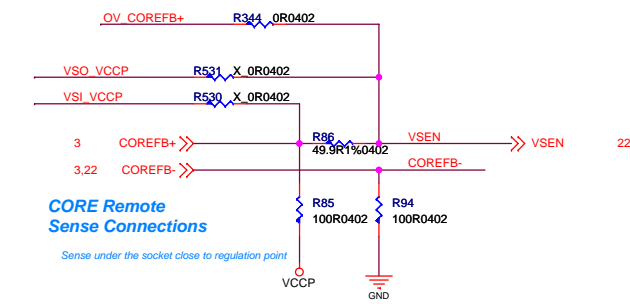
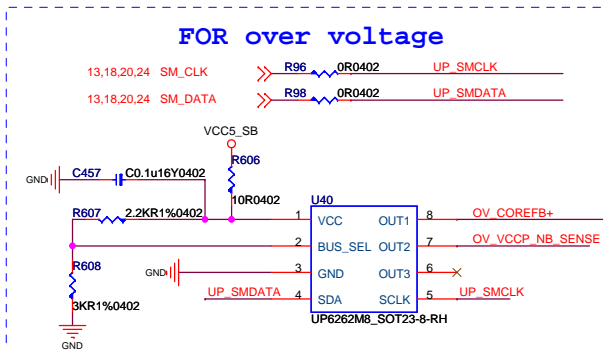
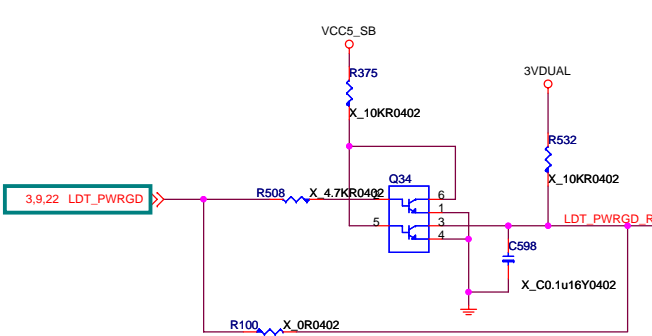
CPU_VDD_RUN



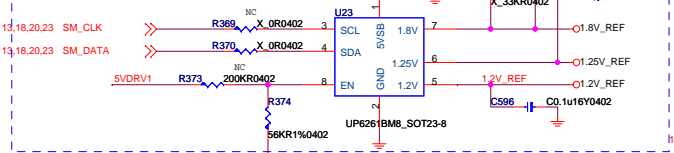
FINTEK75125 : VCCP & VCCP_NB OV



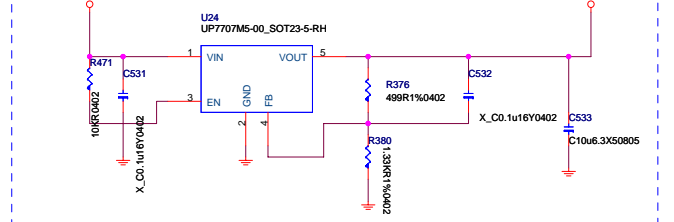
	CPU_VID1	
Parallel VID	Hi	
Serial VID	Low	



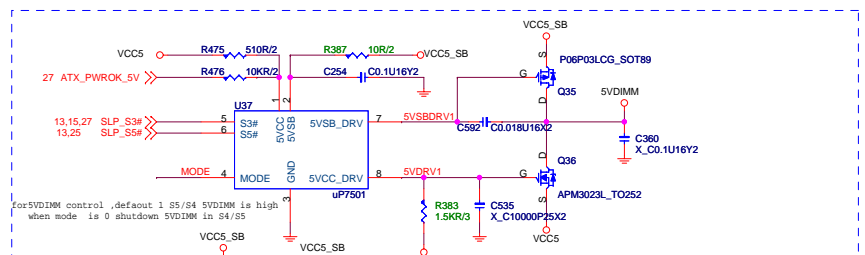
reference Voltage



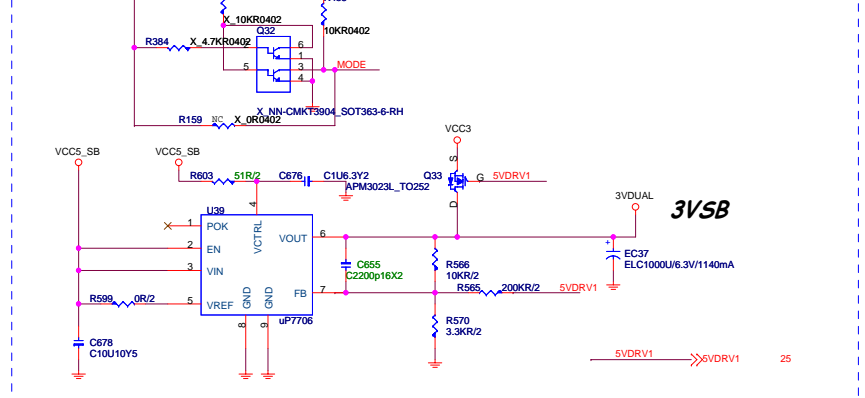
EN PIN for disable and enable 1.2VREF and 1.252REF



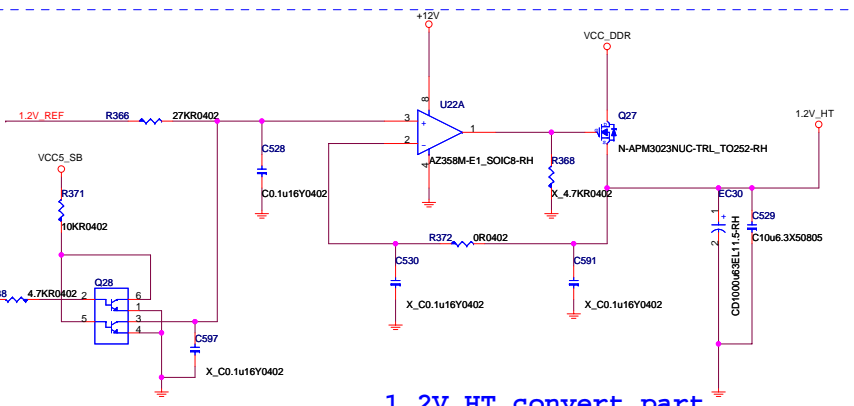
1.1VDUAL convert part



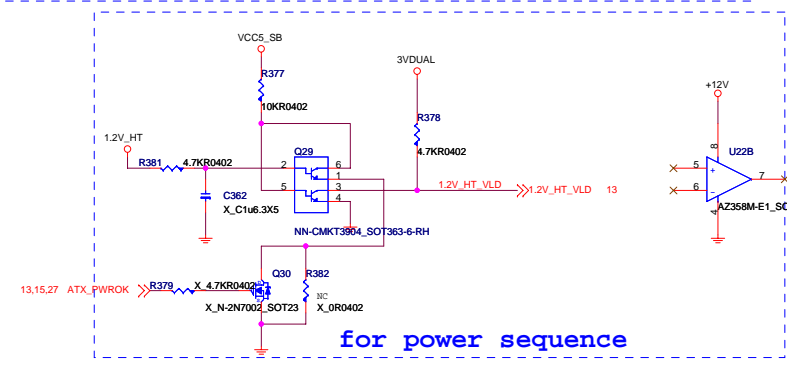
5VDIMM convert part



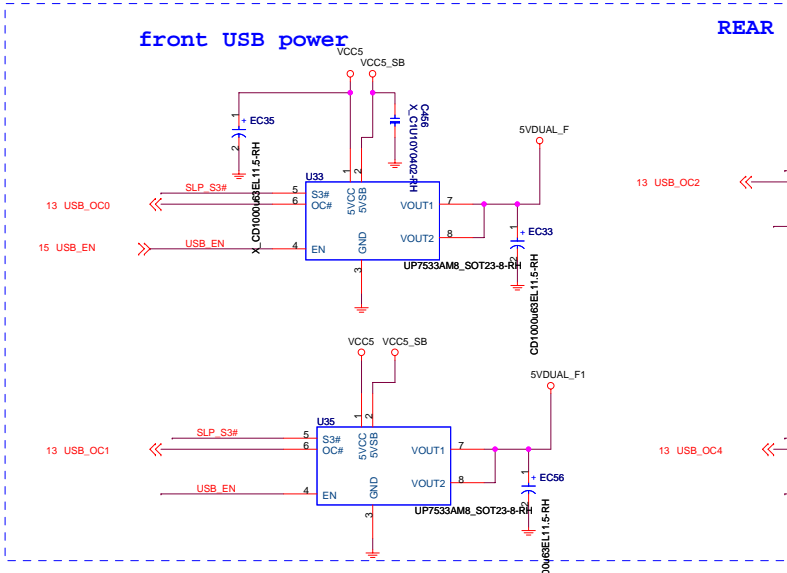
3VSB



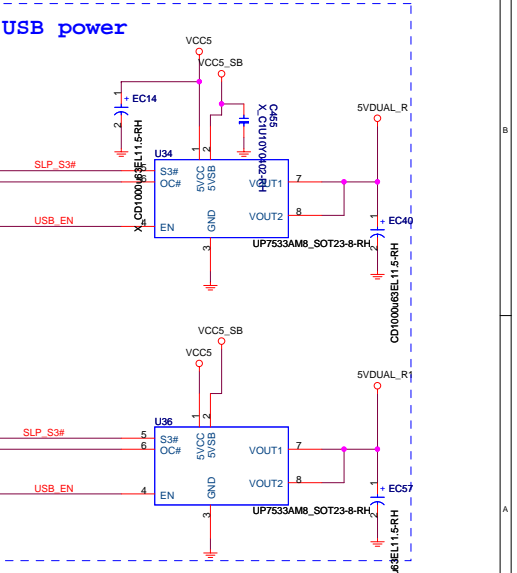
1.2V_HT convert part



for power sequence

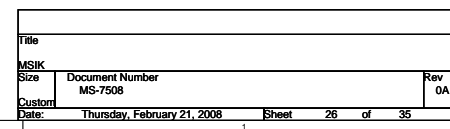
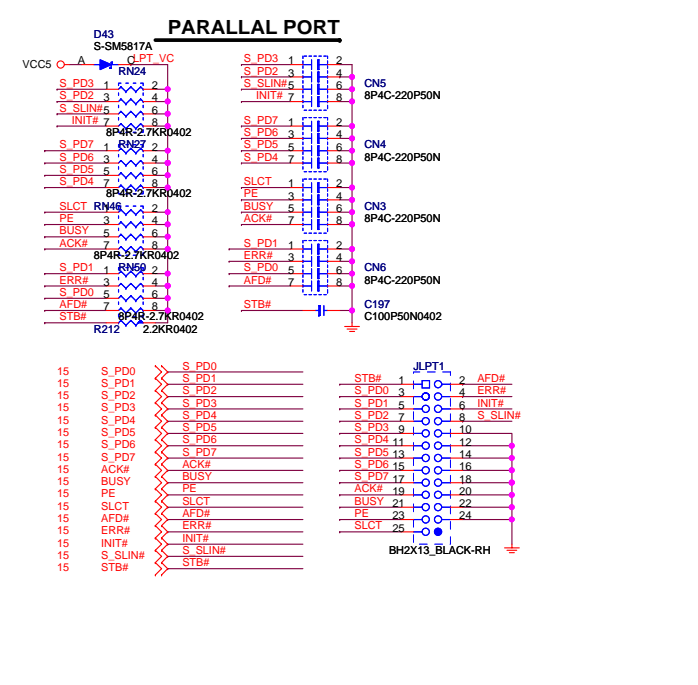


front USB power



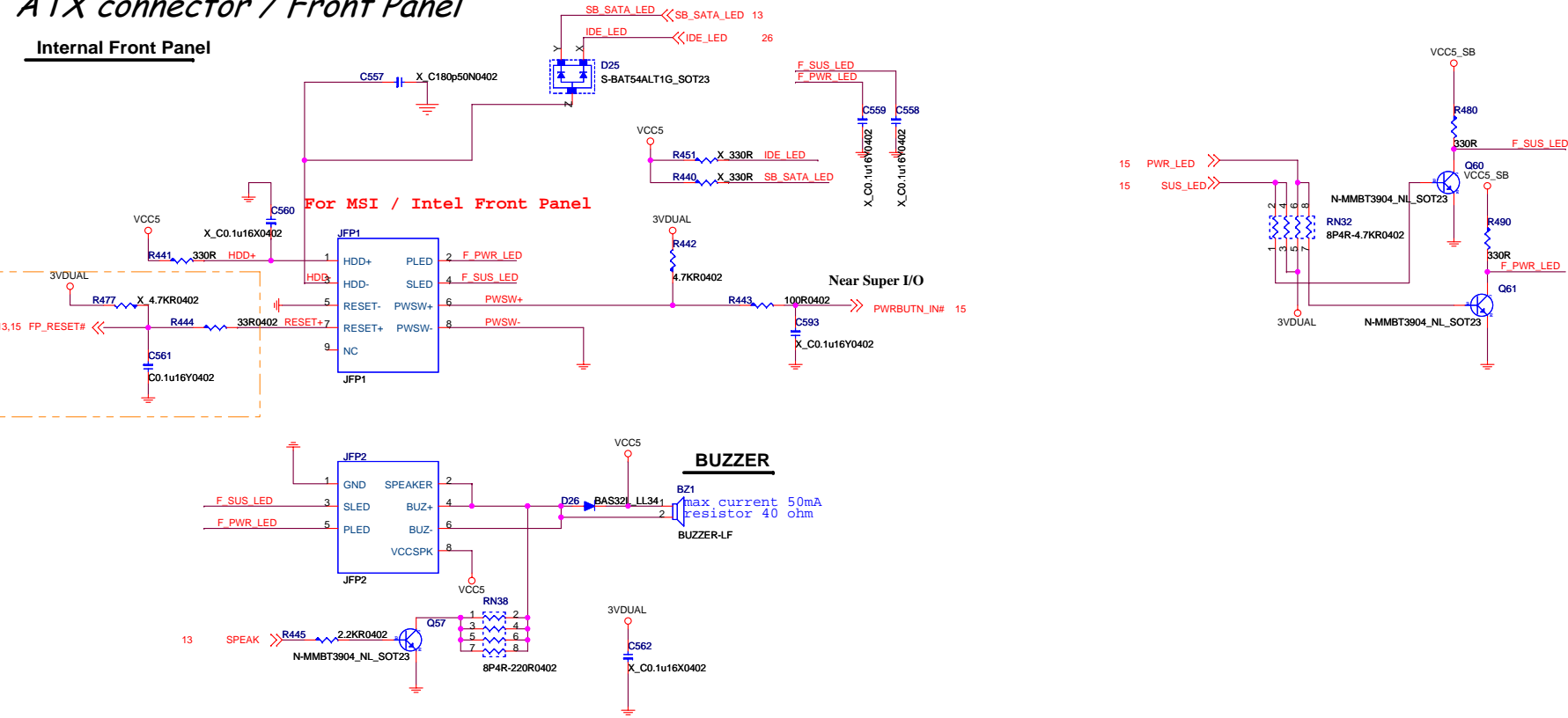
REAR USB power

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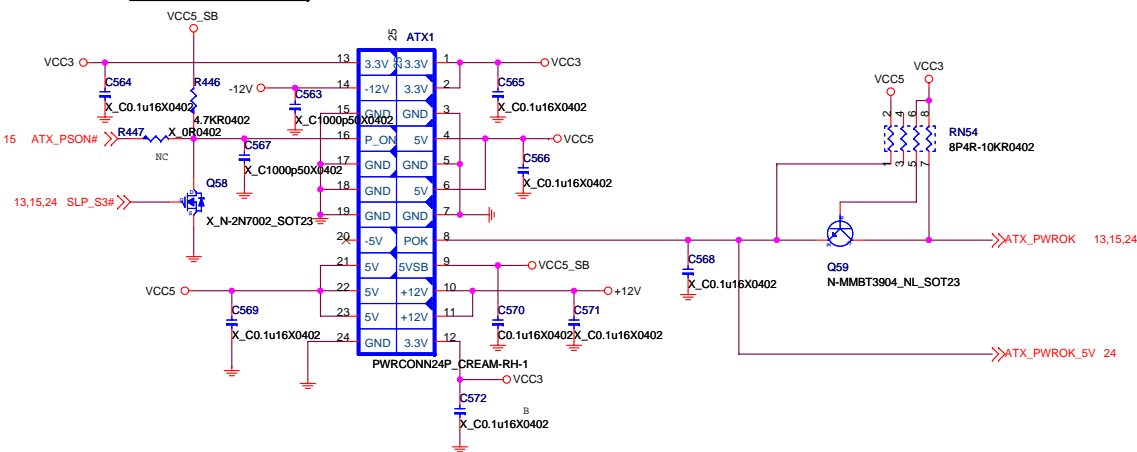


ATX connector / Front Panel

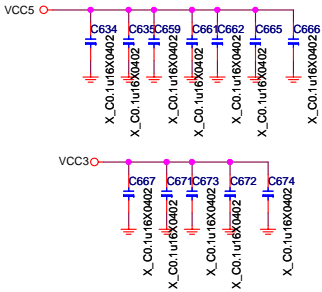
Internal Front Panel



ATX Connector



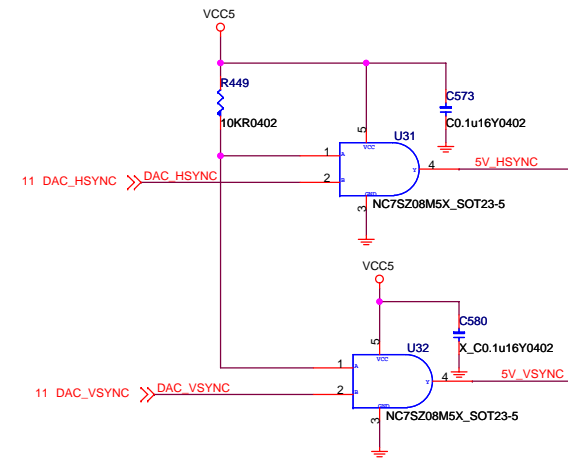
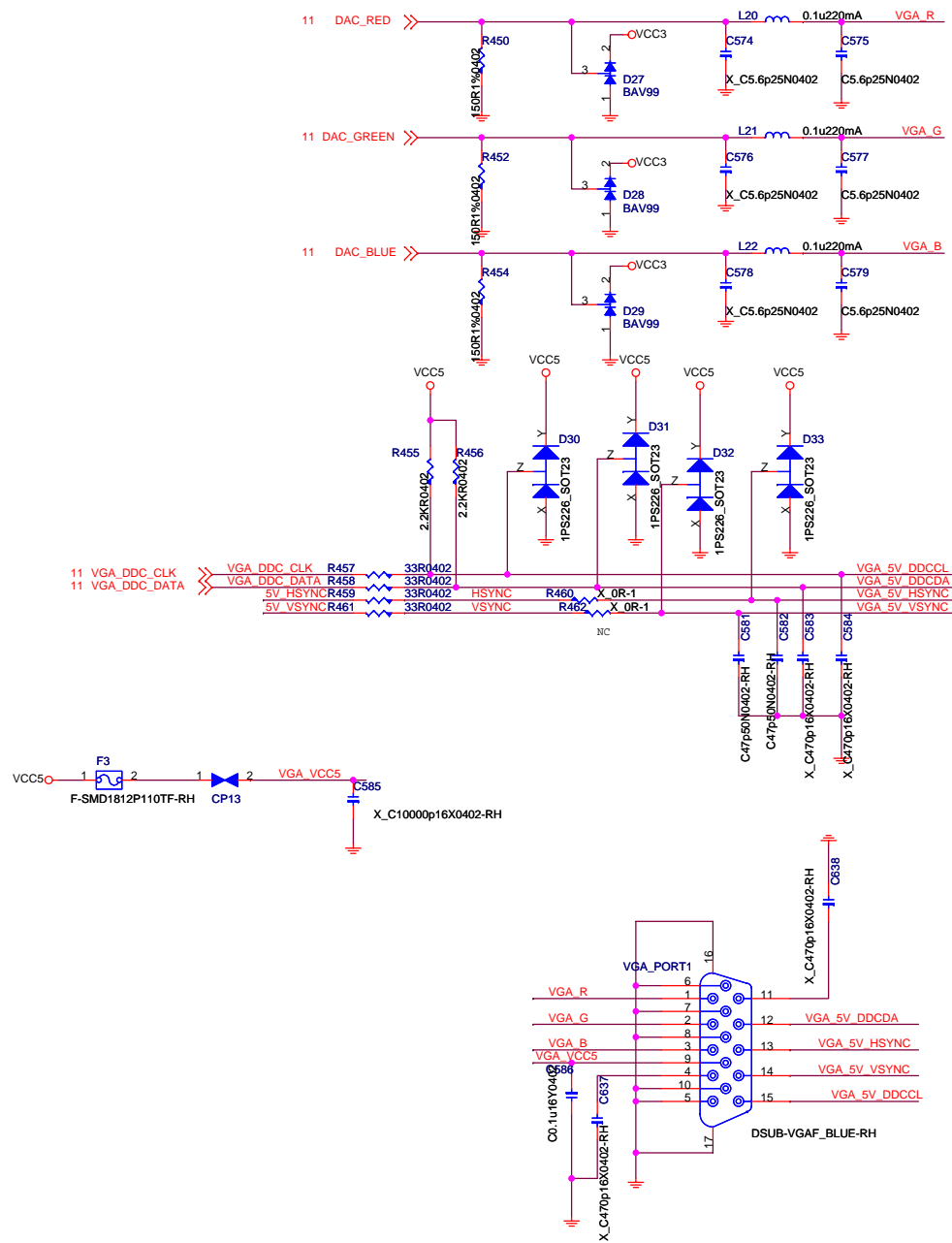
EMI solution



VGA CONNECTOR

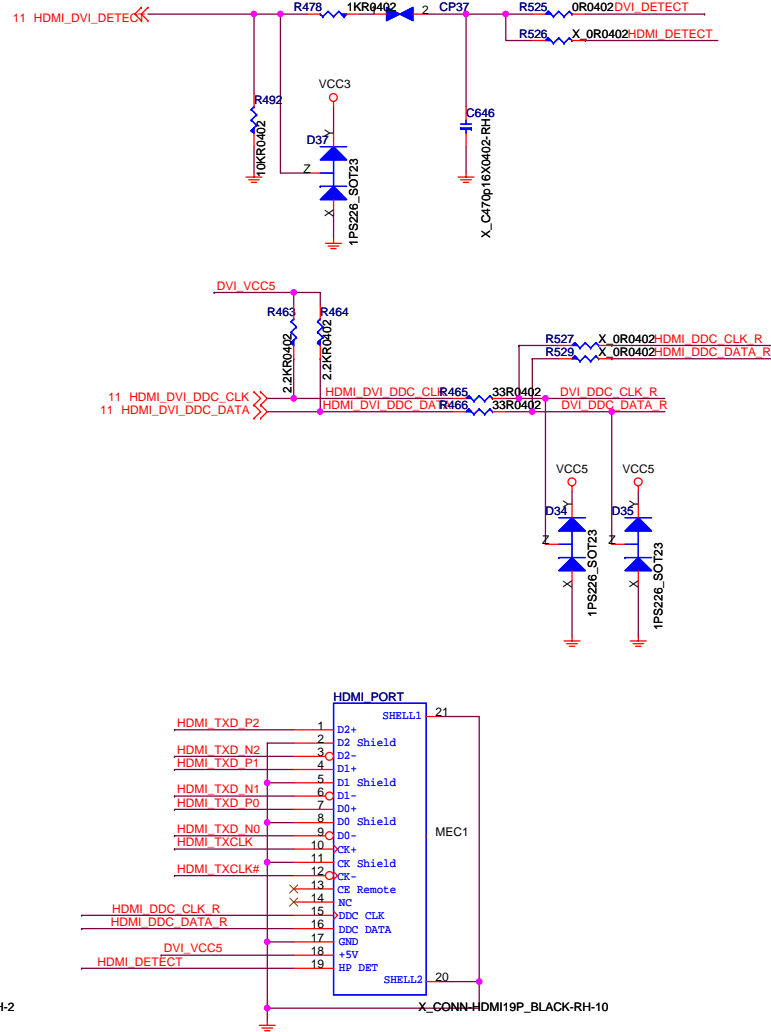
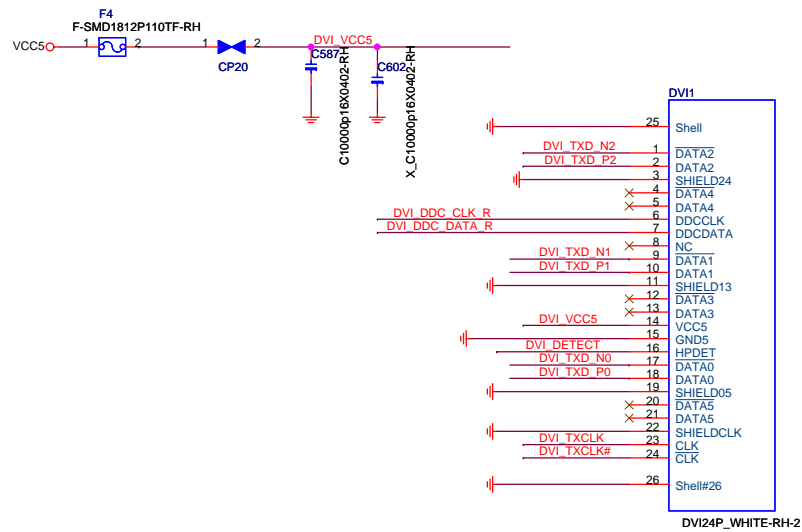
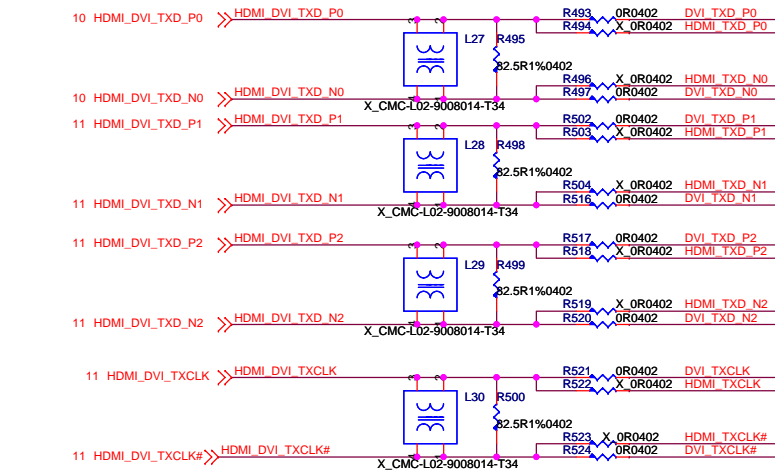
Closed NB


close VGA connector For EMI

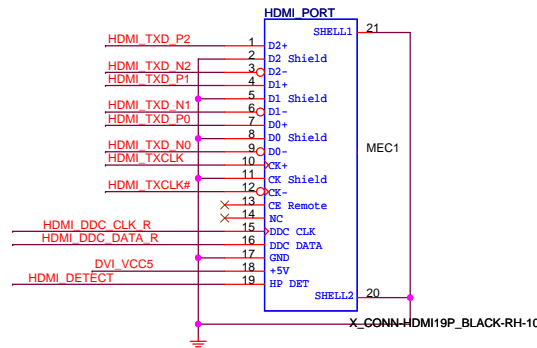


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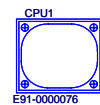
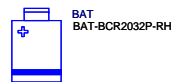
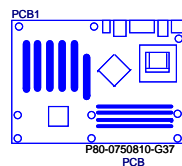
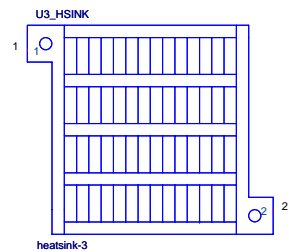
for EMI place near DVI connector



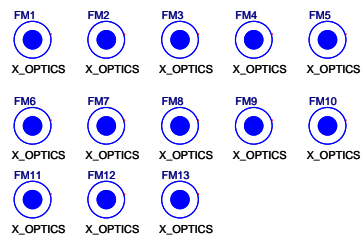
R501  90.9R1%0402
for HDMI EMI used



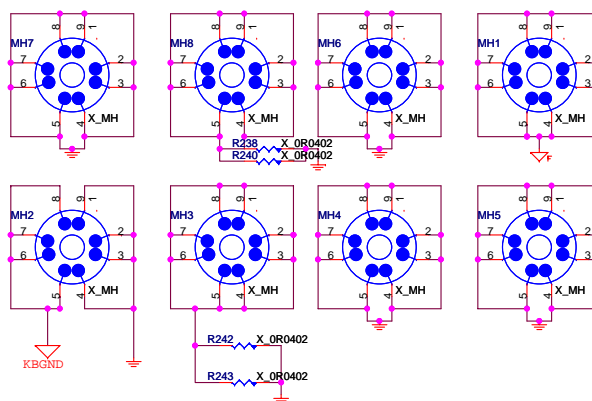
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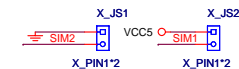
Optics Orientation Holes



Mounting Holes



Simulation



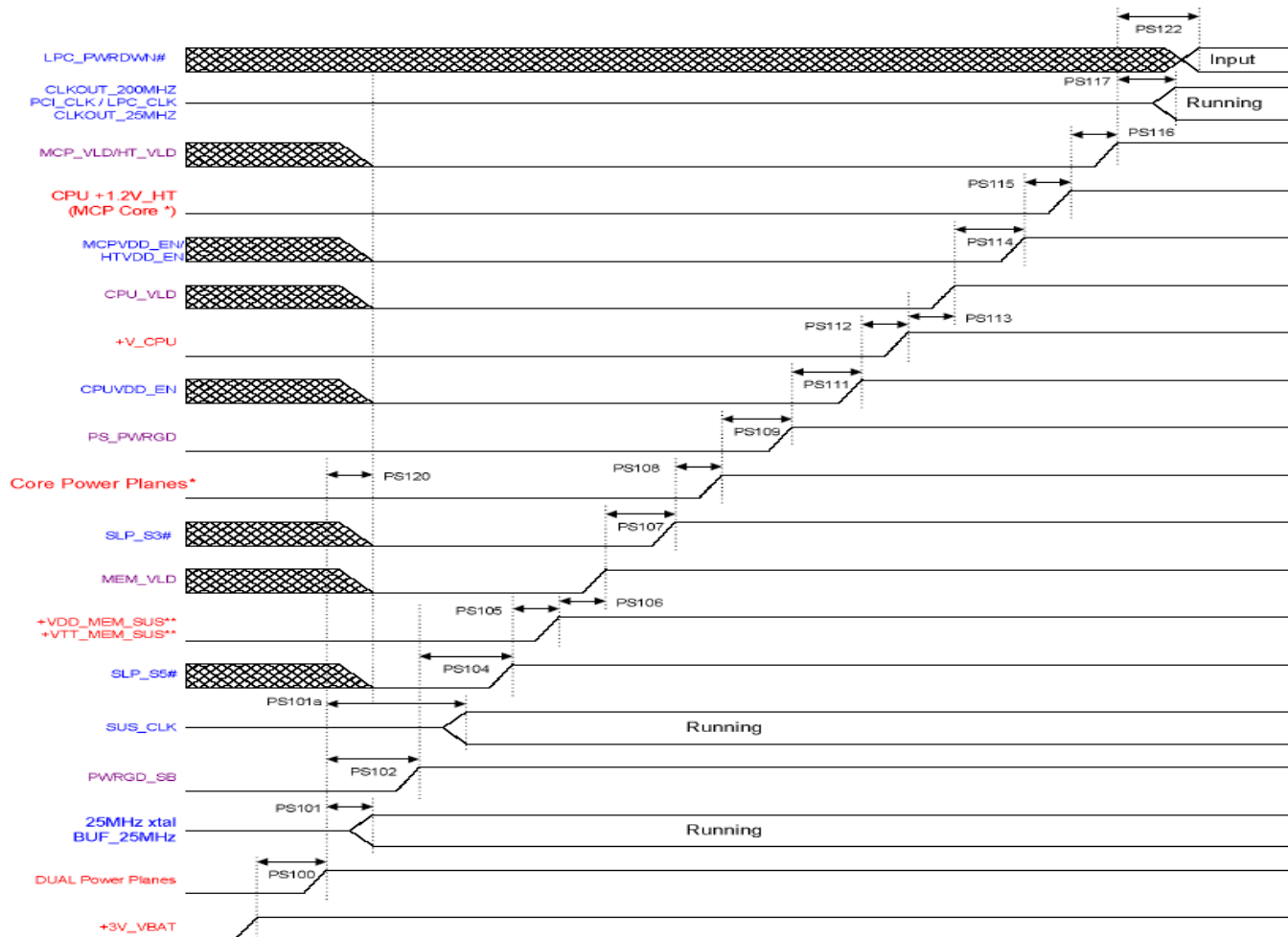
Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7508	MCP78+RTL8211BL+ALC888+2PCI+1PCIEX16+1PCIEX1+2PS2+8USB+2COM+HDMI/DVI/VGA+1Audio+RJ45	Cfg-7508VOA	

MS7508V0A

- 1 page 23 add 1.2vref 1.8 vref 1.25vref capacitor
- 2 add EMI solution
- 3 add R60 C203 for VGA function and change serial induce to82nH
- 4 add EC33 EC40 EC56 EC57 capacitor for SI test fail issue
- 5 remove c250 c251 for sequence issue
- 6 change R309 to 82K as power suggestion
- 7 change VRM_EN circuit
- 8 please 0.1uf near the chipset VBAT power pin
- 9 add EMI parallel port capacitor
- 10 co_lay 75125

change the C193,C195 to 0603
change the R228 to 1.5K
change the R65 to 33 ohm
Add C462,C600
change PWRGD_SBY



Power Planes are in Red MCP output signals are in Blue Motherboard-generated signals to MCP are in Purple

* **Core Power Planes** include:
All power rails without _DUAL or _SUS in the name except:
- CPU Core Power
- CPU +1.2V_HT
- and optionally, the MCP Core voltage rail

** **Memory Power Planes** vary with the memory standard.
- DDR = 2.5, 1.25V
- DDR2 = 1.8, 0.9V
- DDR3 = 1.5, 0.75V

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Date:

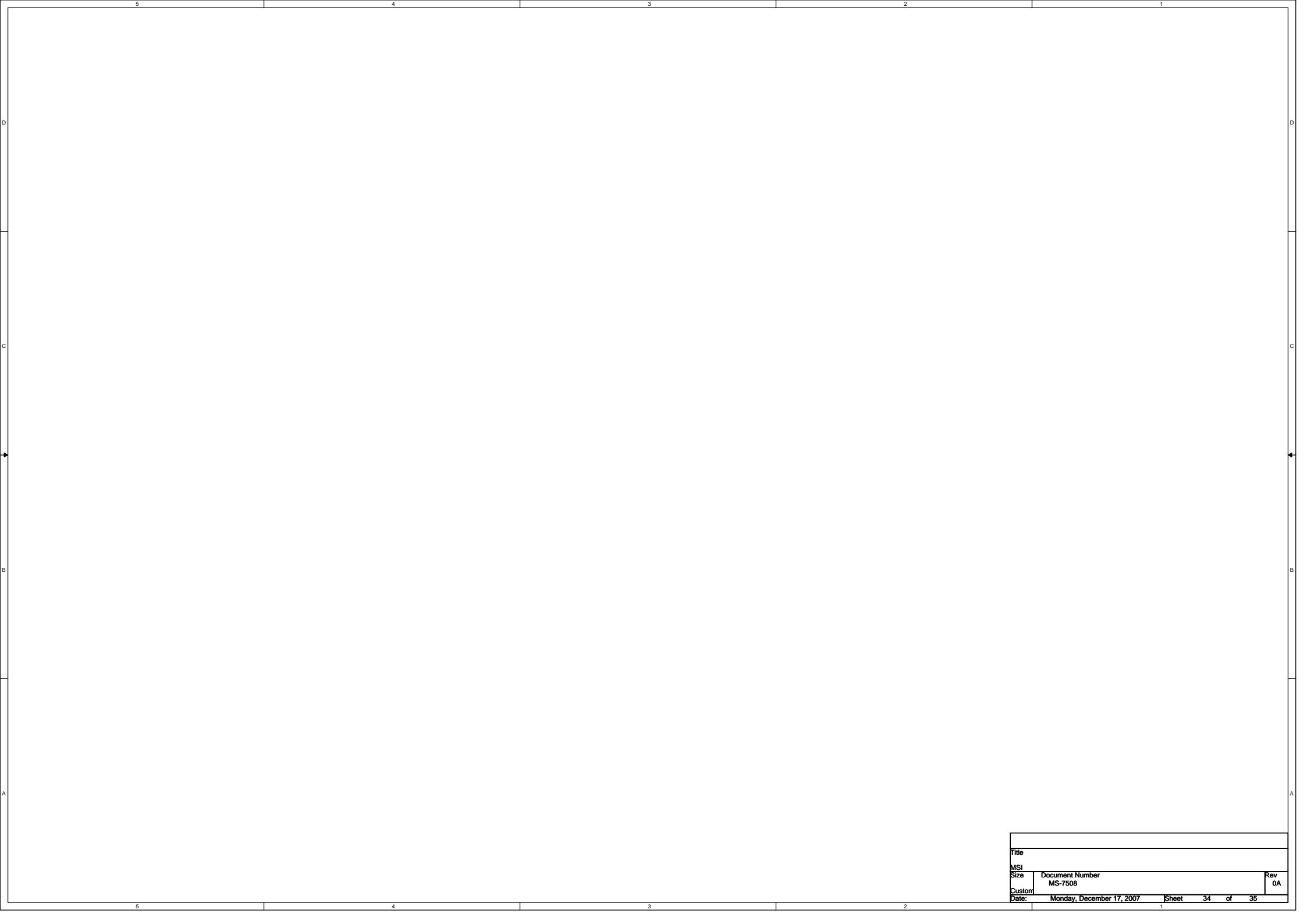
Monday, December 17, 2007

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